

WHAT IS CLAIMED IS:

1        1. A system for providing frequency domain synchronization  
2 for a single carrier signal, said system comprising:

3        a synchronization circuit that is capable of receiving said  
4 single carrier signal, and capable of obtaining a coarse frequency  
5 estimate of said single carrier signal, and capable of obtaining a  
6 fine frequency estimate of said single carrier signal.

1        2. The system as claimed in Claim 1 where said single  
2 carrier signal is a vestigial sideband signal.

1        3. The system as claimed in Claim 1 wherein said  
2 synchronization circuit is capable of obtaining a coarse frequency  
3 estimate of said single carrier signal by locating a pilot carrier  
4 signal on an average power spectrum of said single carrier signal.

1       4. The system as claimed in Claim 1 wherein said  
2 synchronization circuit is capable of obtaining a fine frequency  
3 estimate of said single carrier signal using the frequency error  
4  $\Delta f_p$  where  $\Delta f_p$  is given by the equation:

5       
$$\Delta f_p = [ 1 / (2\pi N T_s) ] [ \text{Arg} [ x_{pr,q}(0) / x_{pr,q+1}(0) ] ]$$

6       where  $[ 1 / (N T_s) ]$  is the frequency spacing, and where  $T_s$  is the  
7 sampling period, and where  $x_{pr}(0)$  is the transmitted signal with  
8 constant frequency error in the zeroth bin, and where  
9  $\text{Arg} [ x_{pr,q}(0) / x_{pr,q+1}(0) ]$  is the phase of a pilot carrier signal  
10 in the zeroth bin.

1       5. The system as claimed in Claim 1 wherein said  
2 synchronization circuit further comprises a three state machine for  
3 obtaining a final frequency estimate of said single carrier signal,  
4 said three state machine capable of obtaining a first frequency  
5 estimate, and capable of obtaining a second frequency estimate with  
6 a known fixed frequency estimate of a positive one fourth bin  
7 spacing, and capable of obtaining a third frequency estimate with a  
8 known fixed frequency estimate of a negative one fourth bin  
9 spacing.

1       6. The system as claimed in Claim 5 wherein said three state  
2 machine is capable of determining which two of the three frequency  
3 estimates are closest in value, and capable of obtaining an  
4 average of the two closest frequency estimates, and capable of  
5 calculating said final frequency estimate of said single carrier  
6 signal by adding one fourth of a bin spacing to said average of the  
7 two closest frequency estimates.

1        7. The system as claimed in Claim 5 where said three state  
2 machine is capable of obtaining said first, second, and third  
3 frequency estimates of a single carrier signal by obtaining a  
4 coarse frequency estimate of said single carrier signal by locating  
5 a pilot carrier signal on an average power spectrum of said single  
6 carrier signal, and by obtaining a fine frequency estimate of said  
7 single carrier signal using the frequency error  $\Delta f_p$  where  $\Delta f_p$  is

8 given by the equation:

9              
$$\Delta f_p = [ 1 / (2\pi N T_s) ] [ \text{Arg} [ X_{pr,q}(0) / X_{pr,q+1}(0) ] ]$$

10        where  $[ 1 / (N T_s) ]$  is the frequency spacing, and where  $T_s$  is the  
11 sampling period, and where  $X_{pr}(0)$  is the transmitted signal with  
12 constant frequency error in the zeroth bin, and where  
13  $\text{Arg} [ X_{pr,q}(0) / X_{pr,q+1}(0) ]$  is the phase of a pilot carrier signal  
14 in the zeroth bin.

1        8. The system as claimed in Claim 7 wherein said  
2 synchronization circuit has a linear transfer function.

1       9. A system for providing frequency domain synchronization  
2 for a single carrier signal, said system comprising:

3       a synchronization circuit comprising a Fast Fourier  
4 Transformer, a coarse frequency estimate circuit coupled to an  
5 output of said Fast Fourier Transformer, and a fine frequency  
6 estimate and phase estimate circuit coupled to an output of said  
7 Fast Fourier Transformer, and

8       a DC estimator circuit capable of being coupled to said fine  
9 frequency estimate and phase estimate circuit in place of said  
10 output of said Fast Fourier Transformer, said DC estimator circuit  
11 capable of providing a time domain DC estimate to said fine  
12 frequency estimate and phase estimate circuit.

1       10. The system as claimed in Claim 9 wherein said  
2 DC estimator circuit calculates said time domain DC estimate, DC  
3 NEW, from the equation:

4               $DC_{NEW} = FFT(0) - Input(N) + Input(0)$

5 where  $FFT(0)$  is a processed DC estimate, and where  $Input(N)$  is an  
6 input sample received N time periods earlier, and where  $Input(0)$  is  
7 a current input sample.

1        11. The system as claimed in Claim 10 wherein said  
2 DC estimator circuit receives the value of Input (N) from an output  
3 of a circular input buffer for said Fast Fourier Transformer, and  
4 wherein said DC estimator circuit receives the value of Input (0)  
5 from an output of a sample rate converter, and wherein said  
6 DC estimator circuit receives the value of FFT(0) from an output of  
7 an adder that adds the outputs of said coarse frequency estimate  
8 circuit and said fine frequency estimate and phase estimate  
9 circuit.

1        12. A method for providing frequency domain synchronization  
2 for a single carrier signal, said method comprising the steps of:  
3            receiving a single carrier signal in a synchronization  
4 circuit;

5            obtaining a coarse frequency estimate of said single carrier  
6 signal in said synchronization circuit; and

7            obtaining a fine frequency estimate of said single carrier  
8 signal in said synchronization circuit.

1        13. The method as claimed in Claim 12 wherein said single  
2 carrier signal is a vestigial sideband signal.

1        14. The method as claimed in Claim 12 where said step of  
2 obtaining a coarse frequency estimate of said single carrier signal  
3 in said synchronization circuit comprises the step of:

4            locating a pilot carrier signal on an average power spectrum  
5 of said single carrier signal.

1        15. The method as claimed in Claim 12 where said step of  
2 obtaining a fine frequency estimate of said single carrier signal  
3 in said synchronization circuit comprises the step of:

4        calculating said fine frequency estimate using the frequency  
5 error  $\Delta f_p$  where  $\Delta f_p$  is given by the equation:

6        
$$\Delta f_p = [ 1 / (2\pi N T_s) ] [ \text{Arg} [ X_{pr,q}(0) / X_{pr,q+1}(0) ] ]$$

7        where  $[ 1 / (N T_s) ]$  is the frequency spacing, and where  $T_s$  is the  
8 sampling period, and where  $X_{pr}(0)$  is the transmitted signal with  
9 constant frequency error in the zeroth bin, and where  
10  $\text{Arg} [ X_{pr,q}(0) / X_{pr,q+1}(0) ]$  is the phase of a pilot carrier signal  
11 in the zeroth bin.

1        16. The method as claimed in Claim 12 further comprising the  
2 steps of:

3        obtaining in a three state machine a first frequency estimate  
4 of said single carrier signal;

5        obtaining in said three state machine a second frequency  
6 estimate of said single carrier signal with a known fixed frequency  
7 estimate of a positive one fourth bin spacing; and

8        obtaining in said three state machine a third frequency

9 estimate of said single carrier signal with a known fixed frequency  
10 estimate of a negative one fourth bin spacing.

1        17. The method as claimed in Claim 16 further comprising the  
2 steps of:

3        determining which two of said three frequency estimates are  
4 closest in value;

5        obtaining an average of the two closest frequency estimates;  
6 and

7        calculating a final frequency estimate of said single carrier  
8 signal by adding one fourth of a bin spacing to said average of the  
9 two closest frequency estimates.

18. The method as claimed in Claim 16 further comprising the steps of:

obtaining said first, second and third frequency estimates of a single carrier signal by

obtaining a coarse frequency estimate of said single carrier signal by locating a pilot carrier signal on an average power spectrum of said single carrier signal; and by

obtaining a fine frequency estimate of said single carrier signal obtaining a fine frequency estimate of said single carrier signal using the frequency error  $\Delta f_p$  where  $\Delta f_p$  is given by the equation:

$$\Delta f_p = [ 1 / (2\pi N T_s) ] [ \text{Arg} [ x_{pr,q}(0) / x_{pr,q+1}(0) ] ]$$

where  $[ 1 / (N T_s) ]$  is the frequency spacing, and where  $T_s$  is the sampling period, and where  $x_{pr}(0)$  is the transmitted signal with constant frequency error in the zeroth bin, and where  $\text{Arg} [ x_{pr,q}(0) / x_{pr,q+1}(0) ]$  is the phase of a pilot carrier signal in the zeroth bin.

19. The method as claimed in Claim 18 wherein said synchronization circuit has a linear transfer function.

1        20. A method for providing frequency domain synchronization  
2 for a single carrier signal, said method comprising the steps of:  
3           generating a time domain DC estimate in a DC estimator  
4 circuit; and  
5           providing said time domain DC estimate to a fine frequency  
6 estimate and phase estimate circuit.

1        21. The method as claimed in Claim 20 wherein said time  
2 domain DC estimate is provided to said fine frequency estimate and  
3 phase estimate circuit by  
4           switching an input of said fine frequency estimate and phase  
5 estimate circuit from an output of a Fast Fourier Transformer to an  
6 output of said DC estimator circuit.

22. The method as claimed in Claim 20 wherein the step of  
generating said time domain DC estimate in said DC estimator  
circuit comprises the step of:

10        calculating said time domain DC estimate, DC<sub>NEW</sub>, from the  
equation:

$$\text{DC}_{\text{NEW}} = \text{FFT}(0) - \text{Input}(N) + \text{Input}(0)$$

where FFT(0) is a processed DC estimate, and where Input(N) is an  
input sample received N time periods earlier, and where Input(0) is  
15 a current input sample.

1        23. The method as claimed in Claim 22 comprising the steps  
2        of:

3            providing the value of Input(N) to said DC estimator circuit  
4        from an output of a circular input buffer for a Fast Fourier  
5        Transformer;

6            providing the value of Input(0) to said DC estimator circuit  
7        from an output of a sample rate converter; and

8            providing the value of FFT(0) from an output of an adder that  
9        adds the outputs of a coarse frequency estimate circuit and said  
10      fine frequency estimate and phase estimate circuit.